AMENDMENTS TO THE SPECIFICATION

Replace the paragraph on page 15 beginning at line 3, with the following new paragraph.

The processor 400 is also operatively coupled to a hardware image processing (HIP) FPGA module 410 such as a Xilinx XCV100E FPGA, and a video head subsystem (VHS) FPGA module 412 such as a Xilinx XCS30XL FPGA which interfaces between the processor 400 and the sensor board 216. It would be apparent to those of ordinary skill in the art that other devices such as an ASIC, a CPLD, a PLD, a dedicated image processing hardware offered by Sumitomo Metals, a processor with FPGA or CPLD structure built in, or the like may be used ~~in~~ instead of the FPGAs. The processor 400 includes a DMA controller 422 as will be explained in more detail below.

Replace the paragraph on page 25 beginning at line 17, with the following new paragraph.

Turning back to Figs. 6 and 7, predefined color register marks 304 and pattern 306 are illustrated. However, as earlier noted, the invention supports the use of programmable color register marks. These marks and patterns can therefore be defined and designed by the ~~used~~ user to suit individual application, and allow flexibility.

"Will be entered" HADN 3/30/04